20 / IDS 2811
E. Phillips
9-10-02

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Yoko HORIGUCHI

Appln. No.: 09/615,705

Confirmation No.: 4487

Filed: July 13, 2000

Docket No: Q60098

Group Art Unit: 2811

Examiner: O. Nadav

For: SEMICONDUCTOR INTEGRATED CIRCUIT

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 and 1.98

Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached PTO/SB/08 A & B (modified) (substitute for PTO Form 1449) form and/or listed herein and which the Examiner may deem material to patentability of the claims of the above-identified application.

1. Japanese Unexamined Patent Application Publication No. 11-154733, published June 8, 1999.

2. Japanese Unexamined Patent Application Publication No. 4-196352, published July 16, 1992.

3. Japanese Unexamined Patent Application Publication No. 7-193195, published July 28, 1995.

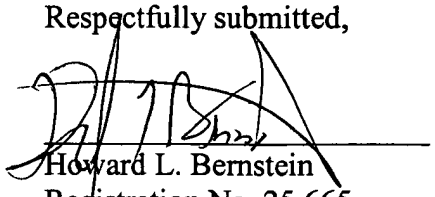
One copy of each of the listed documents is submitted herewith.

The present Information Disclosure Statement is being filed after the later of three months from the application's filing date and the mailing date of the first Office Action on the merits, but before a Final Office Action, Notice of Allowance, or an action that otherwise closes prosecution in the application (whichever is earlier), and therefore Applicant is filing concurrently herewith a Statement Under 37 C.F.R. § 1.97(e). No fee under 37 C.F.R. § 1.17(p) is required.

In compliance with the concise explanation requirement under 37 C.F.R. § 1.98(a)(3) for foreign language documents, Applicant encloses herewith a copy of a Communication from the Japanese Patent Office dated July 16, 2002 in a counterpart application citing such documents, together with an English-language version of that pertinent portion indicating the degree of relevance found by the foreign patent office.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

Respectfully submitted,



Howard L. Bernstein
Registration No. 25,665

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Date: August 27, 2002

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Yoko HORIGUCHI

Appln. No.: 09/615,705

Confirmation No.: 4487

Filed: July 13, 2000

For: SEMICONDUCTOR INTEGRATED CIRCUIT

Docket No: Q60098

Group Art Unit: 2811

Examiner: O. Nadav

STATEMENT UNDER 37 C.F.R. § 1.97(e)

Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned hereby states, upon information and belief:

That each item of information contained in the Information Disclosure Statement filed concurrently herewith was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of said Information Disclosure Statement.

Respectfully submitted,

Howard L. Bernstein
Registration No. 25,665

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Date: August 27, 2002

Ref. Q60098

Annotation (See the List of Cited References, Etc., for the cited references, etc.)

* Claims: 1-3, 8, 10, 12, 14, 18
* Reason 1 or 2
* Cited Reference 1
* Comments

In Cited Reference 1, see the entire document and see the explanations of the figures.

Although Cited Reference 1 does not describe the interconnect resistance of the ground potential interconnection line, it provides a description of laying out static electrical guard elements in the vicinity of MOS capacitors, and thus can be seen to fulfill the size relationships of the interconnect resistances described in Claim 1 of the present application.

Additionally, in relation to Claim 2 of the present application, Cited Reference 1 only describes an example of connecting static electrical guard elements between the ground terminal and an MOS capacitor, and it does not describe an example wherein an MOS capacitor is connected between the ground terminal and an electrostatic guard element. However, in contrast to the ring-shaped power lines and ground lines such as shown in Figure 6 of Cited Reference 1, usually multiple power supply terminals and ground terminals are provided, and thus, in that case, no difference with the invention according to Claim 2 of the present application can be seen. Additionally, no particular difficulty can be seen in switching the layout of the MOS capacitors and the electrostatic guard elements, nor can any particular effects be seen in doing so.

* Claims: 4-6, 9, 11, 13, 15, 16, 17, 19
* Reason 2
* Cited References 1 to 3
* Comments

<Regarding Claims 4-6, 11, 13, 15, and 19>

Although Cited Reference 1 does not describe the aspect of providing electrostatic guard elements on the I/O signal lines, the provision of electrostatic guard elements between the I/O lines and the ground potential lines in order to prevent damage from static electricity is a well-known technology, such as described in, for example, Cited Reference 2.

Additionally, because Cited Reference 1 describes laying out electrostatic guard elements in the vicinity of the MOS capacitors, the distance between the MOS capacitor and the electrostatic guard element equipped between the power line and the ground line should be shorter than the distance between the MOS capacitor and the electrostatic guard element equipped between the I/O signal line and the ground/power lines.

<Regarding Claim 9>

The provision of a power supply voltage transformer circuit when the voltage supplied is different from the operating voltage of the circuit is a well-known technology.

<Regarding Claims 16 and 17>

The use of a thyrister as an electrostatic guard element is a well-known technology, such as described in, for example, Cited Reference 3. (See paragraph [0015].)

List of Cited References, Etc.

1. Unexamined Patent Application Publication H 11-154733
2. Unexamined Patent Application Publication H 04-196352
3. Unexamined Patent Application Publication H 07-193195